

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-193203

(43)Date of publication of application : 03.08.1993

(51)Int.Cl.

B41J 5/30
B41J 29/38
G06F 15/64
H04N 1/387

(21)Application number : 04-031412

(71)Applicant : TOYO ELECTRIC MFG CO LTD

(22)Date of filing : 22.01.1992

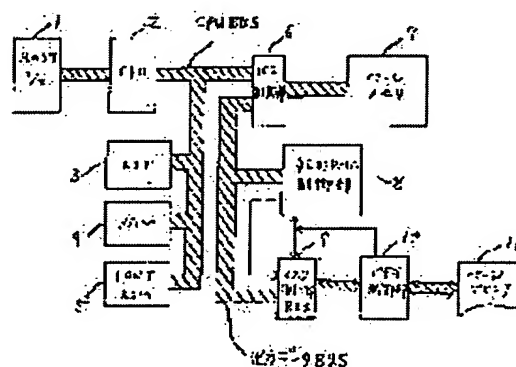
(72)Inventor : TAKEMOTO YOSHINORI
SONOMURA NAGAMASA
BABA ICHIRO

(54) IMAGE RECTANGULAR DMA SYSTEM

(57)Abstract:

PURPOSE: To reduce a burden on a CPU and enhance a total throughput by a method wherein rectangular image data on an arbitrary position of a page memory is transmitted to a printer in a DMA system.

CONSTITUTION: A CPU 2 sets an address of an arbitrary rectangular area on a page memory in a rectangular DMA control part 8 in a bit expression. In the rectangular control part 8, an address and an effective bit are found by a start point and an end point in an X direction. Only data stored in the rectangular area is accessed.



*** NOTICES ***

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1]Picture rectangle DMA system which can carry out the DMA output of the image data created on a page memory by giving arbitrary rectangle parameters in a page printer represented by laser beam printer to a page memory which this page printer has directly at a page printer.

[Claim 2]The picture rectangle DMA system according to claim 1 which expresses a pause of said arbitrary data of a rectangle parameter with bitwise instead of a byte unit, and carries out the DMA transfer of the rectangle data in a fine unit.

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application]This invention can prevent the intervention of a processor (henceforth CPU) as much as possible in a page printer with a page memory, It is related with the DMA system which performs DMA (Direct Memory Access) transmission and enabled it to output fine rectangle data on a page printer by giving arbitrary rectangle parameters for the image data on a page memory.

[0002]

[Description of the Prior Art]The output from the page memory to the conventional page printer, CPU is divided roughly into the method which performs data transfer to the buffer for direct page printers per byte using the method which performs the DMA transfer of an one-line unit via an exclusive DMA controller, or FIFO (first in, first out).

[0003]

[Problem(s) to be Solved by the Invention]However. [whether in the conventional method, when outputting image data to a page printer from a page memory, CPU sets a parameter as an exclusive DMA controller for every line, and] Or the fall of the total throughput was carried out for the method that CPU writes immediate data in printer buffers, such as FIFO. The load of CPU was increasing to the clipping processing of the dot unit for processing in which it writes in on a dummy-spaces memory. This invention is what improved the method to which a printer is made to carry out the DMA transfer of the rectangle data, the fall of a total throughput is prevented and there is a place made into the purpose in reducing the load of CPU.

[0004]

[Means for Solving the Problem]That is, there is a means for attaining the purpose in considering it as DMA system with a rectangle control section which controls only a memory of a tip value of a rectangle given by bitwise of a page memory of a printer, and a termination value.

[0005]

[Function]The tip value of the rectangle to which the image data by which the operation was created on the page memory was given by bitwise from CPU (x_1, y_1), The required bit of parameter x_1 and x_2 is included for the image data which needs a rectangle control section than a termination value (x_2, y_2) from a memory address tip value (x_1, y_1) per byte to a termination value (x_2, y_2). It is possible to transmit without the intervention of CPU from a page memory to the video processing section to a plotter via a system bath at the time of transmission.

[0006]

[Example]Hereafter, one example of this invention is explained in full detail based on a drawing. Drawing 1 is an entire configuration figure for explaining the picture rectangle DMA system of this invention, FONTROM which 1 made the host computer and 2 made CPU and to which, as for ROM and 4, three carried out the memory of the letter symbol for release of drawing, as for RAM and 5, In [as for rectangle direct memory access control and 9, a bus controlling part and 7 are / a video control section and 11 / page printers a mask control register and 10 a page memory and 8 6, and] drawing 1, If the image data outputted by HOST1 to ROM3, RAAM4, and

FONTROM5 is inputted into the page memory 7 by CPU2 via the bus controlling part 6 and the image data for one sheet is completed. The conditions outputted to the page printer 11 are set as the rectangle direct memory access control 8, according to the video requirement signal from the video control section 10, the rectangle direct memory access control 8 begins operation, and required [to a change / via the ** bus controlling part 6 and the mask control register 9] for the page printer 11 in a CPU bus and an output data bus — image data transfer is carried out. [0007]Next, by giving the arbitrary rectangle parameters made into the gist of this invention explains the method which carries out the DMA output of the picture created on the page memory 7 directly at the page printer 11 based on drawing 1, referring to drawing 2 (a), (b), (c), drawing 3, and drawing 4. In [drawing 2 (a), (b), and (c) is an explanatory view showing the example of the page memory 7, and] a figure (a), The image data for one sheet outputted by CPU2 is shown, and The peak value of the page memory 7 (0, 0), What is necessary is to transmit only this shadow area 7a to the page printer 11, if it is a termination value (x_e, y_e), a tip value (x_1, y_1) of the rectangle which gave the slash, and a termination value (x_2, y_2). Usually, although it is **** to which this shadow area 7a is transmitted by the page printer 11 by CPU per byte, In this invention, moreover, it transmits to the page printer 11 by bitwise, and this transmission is not based on CPU, but by instructions of the video control section 10, the rectangle direct memory access control 8 begins to operate, and the shadow area 7a is transmitted to the page printer 11.

[0008]The explanation transmitted by this bitwise is explained based on a figure (b) and (c). A figure (b) shows the invalidity to 1 byte of a tip value (x_1, y_1) (it is henceforth called a tip address), and the number of effective bits, and a figure (c) shows the invalidity to 1Byte of a termination value (x_2, y_2) (it is henceforth called an end address), and the number of effective bits. Usually, the validity in 1 byte since a DMA transfer is 1 byte, 2 bytes, or 4 bytes and 1 byte is 8 bits and the number of invalid bits, When an invalid bit is set to alpha, when $= (x_1/8) n_1 - (\alpha/8)$ and the number of effective bits are set to beta, drawing 2 (c) is shown by $= (x_2/8) n_2 - (\beta/8)$ in drawing 2 (b). Here, n_1 shows the tip address in arbitrary values, and the end address in values with arbitrary n_2 .

[0009]On the upper page memory, these addresses are actually expressed with tip address $(x_e+1) y_1+n_1$ and end address $(x_e+1) y_2+n_2$. However, in the case of $\alpha \neq 0$ and $\beta \neq 0$, about a x direction, the number of effective bits of the address of x_1 and x_2 is set to beta respectively $(8-\alpha)$. In the case of $\beta = 0$, it is set to end address $(x_e+1) y_2+n_2-1$. When a MASK byte expresses here the invalid bit of 0–7 bits of data which comprises 1 byte (8 bits) with a binary system, Since all binary systems can be expressed by a low rank (side which went to 0 bit directions from 7-bit side when x_e direction address of drawing 1 is 0, 1, and 2.....7 bits is shown) triplet, a triplet is needed. Thus, although it is a translation in which a DMA transfer is carried out to the page printer 11 by operation of the rectangle direct memory access control 8 by fine bitwise, a logic circuit explains the operation below.

[0010]Drawing 3 is a block diagram of the rectangle direct memory access control of x, and The tip address of the rectangular shadow area 7a (x_1, y_1), A set of an end address (x_2, y_2) and end address x_e of the page memory 7 will change DMA into Byte with each dividers 12 and 16 first for Byte transmission. About low rank 3 Bit of low rank 3 Bit ($x_2/8$) of each MASK Bit ($x_1/8$), as drawing 1 explained, it is used for processing of the number of effective bits. However, in order to process the above-mentioned termination Adlai $*(x_e+1) y_2+n_2-1$ with the subtractor 18 in the case of low rank 3 Bit=0 of ($x_2/8$), the value of $x_2/(8)-1$ is set to the comparator 19. And if GOF/F which is a seizing signal is set to this control section from CPU and XCLK which is an image synchronizing signal is inputted from the video control section 10, The counter 14 moves and it is searched [of a x direction] whether a counter value is larger [by the comparator 13]

in effective value than $(x_1/8)$, or equal. If the value of the x counter 14 becomes equal to x_e , the Y counter 20 will be counted up one time. The effective value of the direction of Y also becomes effective by whether a counter value is larger than y_1 or equal by the comparator 21. And the terminal point of a x direction is detected by the comparator 19. The terminal point of Y_2 is similarly detected by the Y_2 comparator 22.

[0011]The shadow area 7a which is the effective value of drawing 1 as mentioned above is detected. In order that the value of x counter and Y counter may become Lower and a Upper address respectively in the address to the page memory 7 or a memory read signal may not come only out of the above-mentioned useful range in the memory read control part 23, the total throughput of CPU improves also at this point. Drawing 4 is a block diagram which determines the starting point of the x direction shown by drawing 1, and the effective bits of an end part, and, in the case of the starting point, a low rank triplet, In order to change into 8 bits, it is inputted into the mask 24 in the timing of x and MSKSET, and it is reversed (effective-bits 8-alpha), and an output is set in the register 30 by the 8-bit register 30 in the timing of an iolite signal (I/OW) through the gate of the gate circuit 25. When X_1 MSKSET is an imitation, it is set in the register 30 through the gate circuit 26 (when it is not the starting point of a x direction). In the case of the terminal point of a x direction, a low rank $(x_2/8)$ triplet is changed into 8 bits through the mask 27 in the timing of X_2 MSK, and an output remains as it is and is set in the register 30 through the gate circuit (effective-bits beta) 28. When X_2 MSKSET is an imitation (it is not a terminal point of a x direction), it is set in the register 30 through the gate circuit 25.

[0012]

[Effect of the Invention]As explained above, according to this invention, the DMA transfer of the data created without the intervention of CPU on the page memory from the page memory for page printers can be carried out to a page printer at high speed, And in order to access the data of only a required rectangle portion on a page memory, a total throughput becomes large extremely. Since a pause of the data of arbitrary rectangle parameters is not a byte unit but bitwise and clipping of a dot unit of it becomes possible in hard, it can decrease the load of a total throughput and CPU.

[0013]

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.*** shows the word which can not be translated.

3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Industrial Application]This invention can prevent the intervention of a processor (henceforth CPU) as much as possible in a page printer with a page memory, It is related with the DMA system which performs DMA (Direct Memory Access) transmission and enabled it to output fine rectangle data on a page printer by giving arbitrary rectangle parameters for the image data on a page memory.

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art]The output from the page memory to the conventional page printer, CPU is divided roughly into the method which performs data transfer to the buffer for direct page printers per byte using the method which performs the DMA transfer of an one-line unit via an exclusive DMA controller, or FIFO (first in, first out).

[Translation done.]

*** NOTICES ***

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention]As explained above, according to this invention, the DMA transfer of the data created without the intervention of CPU on the page memory from the page memory for page printers can be carried out to a page printer at high speed, And in order to access the data of only a required rectangle portion on a page memory, a total throughput becomes large extremely. Since a pause of the data of arbitrary rectangle parameters is not a byte unit but bitwise and clipping of a dot unit of it becomes possible in hard, it can decrease the load of a total throughput and CPU.

[Translation done.]

* NOTICES *

JP0 and INPIT are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However. [whether in the conventional method, when outputting image data to a page printer from a page memory, CPU sets a parameter as an exclusive DMA controller for every line, and] Or the fall of the total throughput was carried out for the method that CPU writes immediate data in printer buffers, such as FIFO. The load of CPU was increasing to the clipping processing of the dot unit for processing in which it writes in on a dummy-spaces memory. This invention is what improved the method to which a printer is made to carry out the DMA transfer of the rectangle data, the fall of a total throughput is prevented and there is a place made into the purpose in reducing the load of CPU.

[Translation done.]

*** NOTICES ***

JPO and INPIT are not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

MEANS

[Means for Solving the Problem]That is, there is a means for attaining the purpose in considering it as DMA system with a rectangle control section which controls only a memory of a tip value of a rectangle given by bitwise of a page memory of a printer, and a termination value.

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

OPERATION

[Function]The tip value of the rectangle to which the image data by which the operation was created on the page memory was given by bitwise from CPU (x_1, y_1). The required bit of parameter x_1 and x_2 is included for the image data which needs a rectangle control section than a termination value (x_2, y_2) from a memory address tip value (x_1, y_1) per byte to a termination value (x_2, y_2). It is possible to transmit without the intervention of CPU from a page memory to the video processing section to a plotter via a system bath at the time of transmission.

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

- 1.This document has been translated by computer. So the translation may not reflect the original precisely.
- 2.**** shows the word which can not be translated.
- 3.In the drawings, any words are not translated.

EXAMPLE

[Example] Hereafter, one example of this invention is explained in full detail based on a drawing. Drawing 1 is an entire configuration figure for explaining the picture rectangle DMA system of this invention, FONTROM which 1 made the host computer and 2 made CPU and to which, as for ROM and 4, three carried out the memory of the letter symbol for release of drawing, as for RAM and 5, In [as for rectangle direct memory access control and 9, a bus controlling part and 7 are / a video control section and 11 / page printers a mask control register and 10 a page memory and 8 6, and] drawing 1. If the image data outputted by HOST1 to ROM3, RAAM4, and FONTROM5 is inputted into the page memory 7 by CPU2 via the bus controlling part 6 and the image data for one sheet is completed, The conditions outputted to the page printer 11 are set as the rectangle direct memory access control 8, according to the video requirement signal from the video control section 10, the rectangle direct memory access control 8 begins operation, and required [to a change / via the ** bus controlling part 6 and the mask control register 9] for the page printer 11 in a CPU bus and an output data bus -- image data transfer is carried out. [0007] Next, by giving the arbitrary rectangle parameters made into the gist of this invention explains the method which carries out the DMA output of the picture created on the page memory 7 directly at the page printer 11 based on drawing 1, referring to drawing 2 (a), (b), (c), drawing 3, and drawing 4. In [drawing 2 (a), (b), and (c) is an explanatory view showing the example of the page memory 7, and] a figure (a), The image data for one sheet outputted by CPU2 is shown, and The peak value of the page memory 7 (0, 0), What is necessary is to transmit only this shadow area 7a to the page printer 11, if it is a termination value (x_e, y_e), a tip value (x_1, y_1) of the rectangle which gave the slash, and a termination value (x_2, y_2). Usually, although it is **** to which this shadow area 7a is transmitted by the page printer 11 by CPU per byte, In this invention, moreover, it transmits to the page printer 11 by bitwise, and this transmission is not based on CPU, but by instructions of the video control section 10, the rectangle direct memory access control 8 begins to operate, and the shadow area 7a is transmitted to the page printer 11.

[0008] The explanation transmitted by this bitwise is explained based on a figure (b) and (c). A figure (b) shows the invalidity to 1 byte of a tip value (x_1, y_1) (it is henceforth called a tip address), and the number of effective bits, and a figure (c) shows the invalidity to 1Byte of a termination value (x_2, y_2) (it is henceforth called an end address), and the number of effective bits. Usually, the validity in 1 byte since a DMA transfer is 1 byte, 2 bytes, or 4 bytes and 1 byte is 8 bits and the number of invalid bits, When an invalid bit is set to alpha, when $= (x_1/8) n_1 - (\alpha/8)$ and the number of effective bits are set to beta, drawing 2 (c) is shown by $= (x_2/8) n_2 - (\beta/8)$ in drawing 2 (b). Here, n_1 shows the tip address in arbitrary values, and the end address in values with arbitrary n_2 .

[0009] On the upper page memory, these addresses are actually expressed with tip address (x_e+1) y_1+n_1 and end address (x_e+1) y_2+n_2 . However, in the case of $\alpha \neq 0$ and $\beta \neq 0$, about a x direction, the number of effective bits of the address of x_1 and x_2 is set to beta respectively

(8-alpha). In the case of $\beta = 0$, it is set to end address $(x_e + 1) y_2 + n_2 - 1$. When a MASK byte expresses here the invalid bit of 0-7 bits of data which comprises 1 byte (8 bits) with a binary system, Since all binary systems can be expressed by a low rank (side which went to 0 bit directions from 7-bit side when x_e direction address of drawing 1 is 0, 1, and 2.....7 bits is shown) triplet, a triplet is needed. Thus, although it is a translation in which a DMA transfer is carried out to the page printer 11 by operation of the rectangle direct memory access control 8 by fine bitwise, a logic circuit explains the operation below.

[0010] Drawing 3 is a block diagram of the rectangle direct memory access control of x , and The tip address of the rectangular shadow area 7a (x_1, y_1), A set of an end address (x_2, y_2) and end address x_e of the page memory 7 will change DMA into Byte with each dividers 12 and 16 first for Byte transmission. About low rank 3 Bit of low rank 3 Bit ($x_2/8$) of each MASK Bit ($x_1/8$), as drawing 1 explained, it is used for processing of the number of effective bits. However, in order to process the above-mentioned termination Adlai $((x_e + 1) y_2 + n_2 - 1)$ with the subtractor 18 in the case of low rank 3 Bit=0 of ($x_2/8$), the value of $x_2/(8) - 1$ is set to the comparator 19. And if GOF/F which is a seizing signal is set to this control section from CPU and XCLK which is an image synchronizing signal is inputted from the video control section 10, The counter 14 moves and it is searched [of a x direction] whether a counter value is larger [by the comparator 13] in effective value than ($x_1/8$), or equal. If the value of the x counter 14 becomes equal to x_e , the Y counter 20 will be counted up one time. The effective value of the direction of Y also becomes effective by whether a counter value is larger than y_1 or equal by the comparator 21. And the terminal point of a x direction is detected by the comparator 19. The terminal point of Y_2 is similarly detected by the Y_2 comparator 22.

[0011] The shadow area 7a which is the effective value of drawing 1 as mentioned above is detected. In order that the value of x counter and Y counter may become Lower and a Upper address respectively in the address to the page memory 7 or a memory read signal may not come only out of the above-mentioned useful range in the memory read control part 23, the total throughput of CPU improves also at this point. Drawing 4 is a block diagram which determines the starting point of the x direction shown by drawing 1, and the effective bits of an end part, and, in the case of the starting point, a low rank triplet, In order to change into 8 bits, it is inputted into the mask 24 in the timing of x and MSKSET, and it is reversed (effective-bits 8-alpha), and an output is set in the register 30 by the 8-bit register 30 in the timing of an iolite signal (I/OW) through the gate of the gate circuit 25. When X_1 MSKSET is an imitation, it is set in the register 30 through the gate circuit 26 (when it is not the starting point of a x direction). In the case of the terminal point of a x direction, a low rank ($x_2/8$) triplet is changed into 8 bits through the mask 27 in the timing of X_2 MSK, and an output remains as it is and is set in the register 30 through the gate circuit (effective-bits β) 28. When X_2 MSKSET is an imitation (it is not a terminal point of a x direction), it is set in the register 30 through the gate circuit 25.

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]Drawing 1 is an imaged figure of a page memory where effective image data is stored.

[Drawing 2]Drawing 2 (a), (b), and (c) is a block diagram showing the composition of the picture rectangle DMA transfer method of this example.

[Drawing 3]Drawing 3 is a block diagram which performs the rectangle DMA control and the page memory address generation in an example.

[Drawing 4]Drawing 4 is a block diagram which determines the effective bits of the starting point of the x direction on the page memory in an example, and a terminal point.

[0014]

[Description of Notations]

1 Host computer

2 CPU

3 ROM

4 RAM

5 FONTROM

6 Bus controlling part

7 Page memory

8 Rectangle direct memory access control

9 Mask control register

10 Video control section

11 Page printer

[Translation done.]

* NOTICES *

JPO and INPIT are not responsible for any damages caused by the use of this translation.

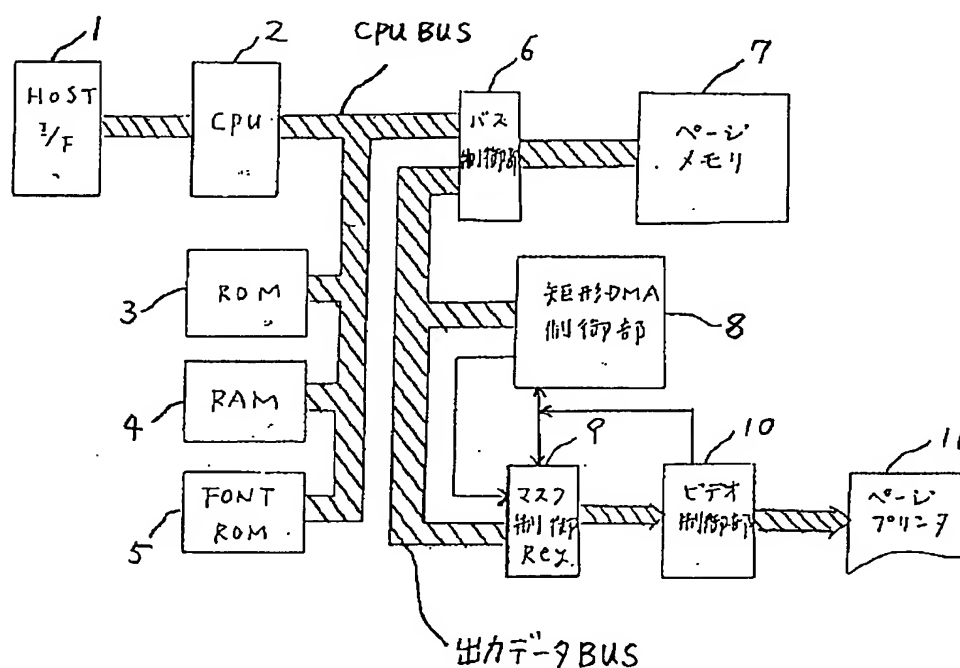
1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.*** shows the word which can not be translated.

3.In the drawings, any words are not translated.

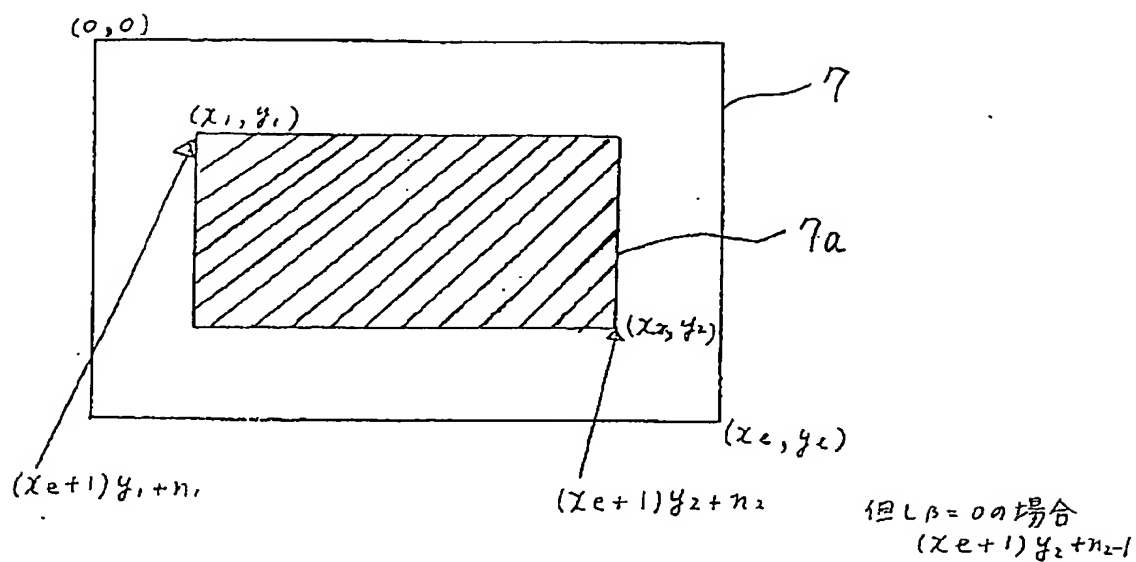
DRAWINGS

[Drawing 1]

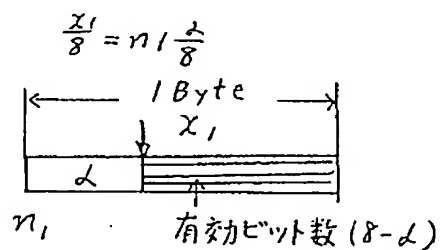


[Drawing 2]

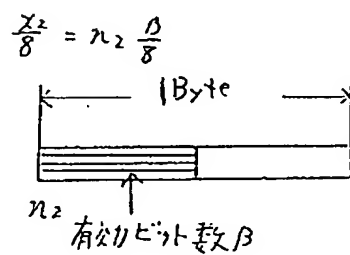
(a)



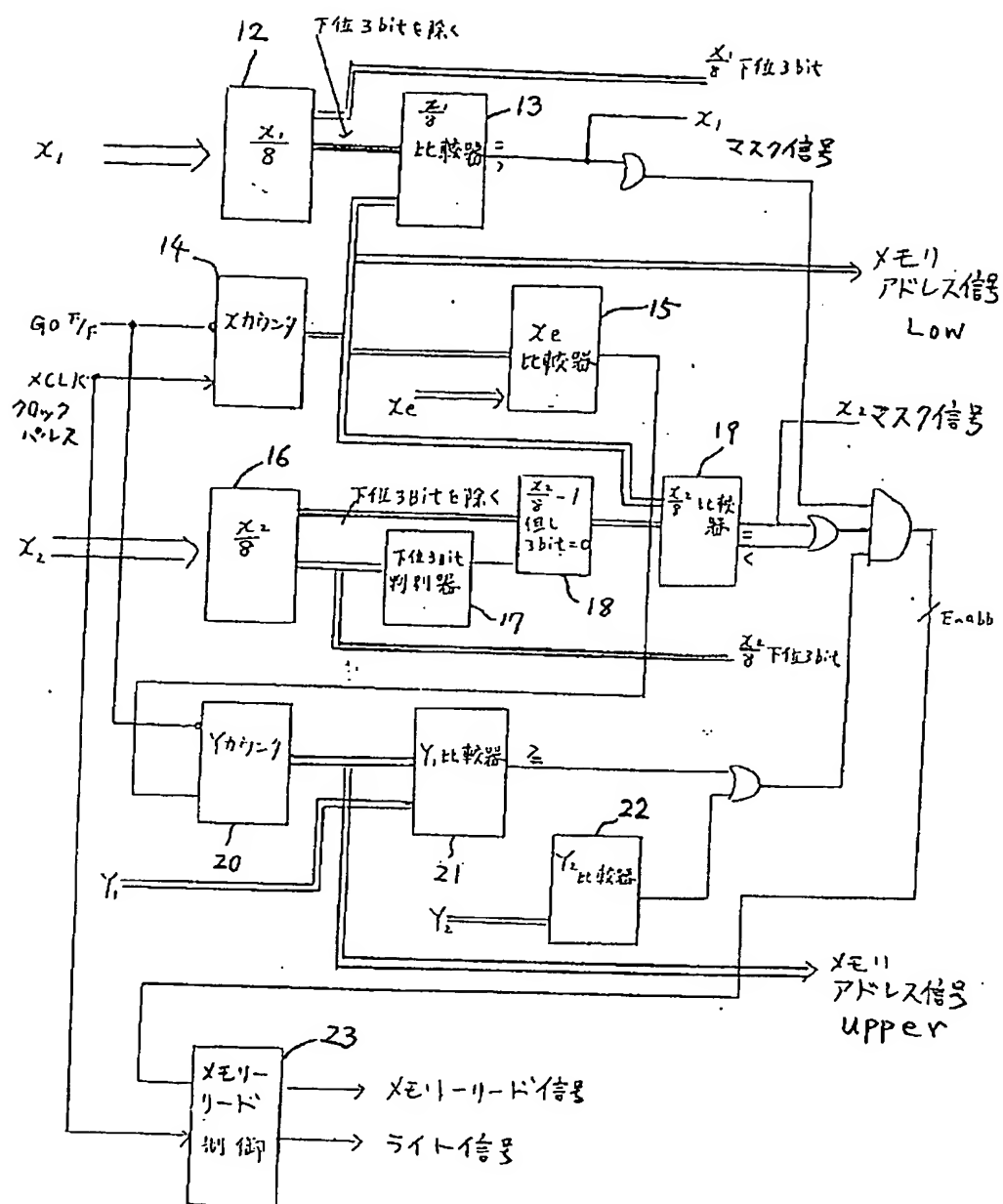
(b)



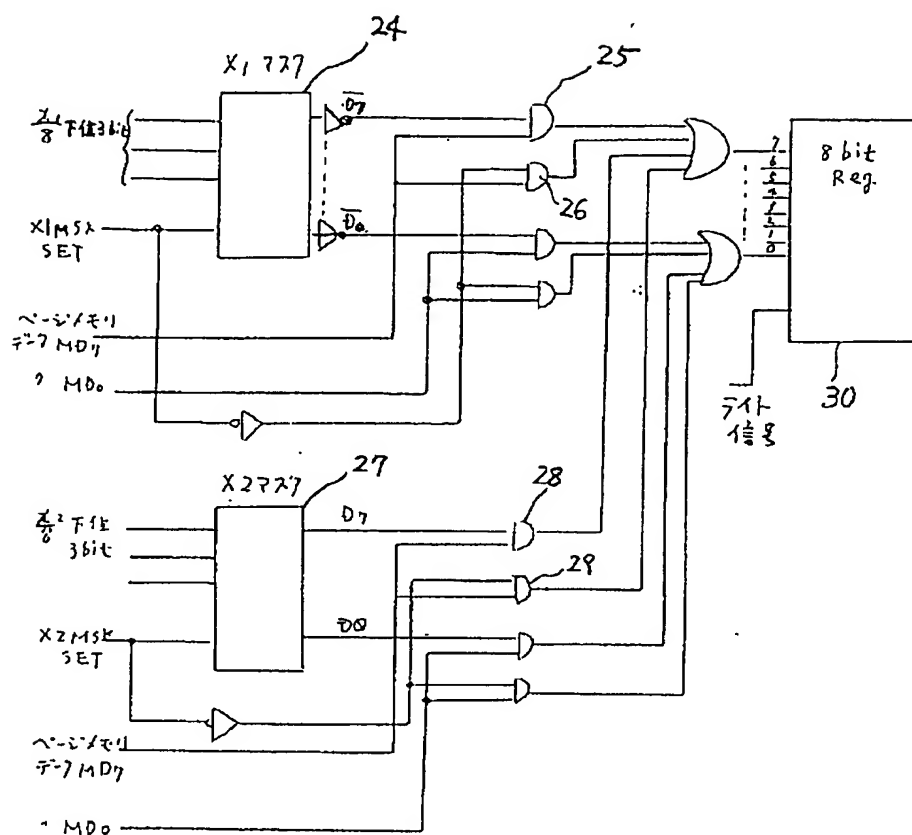
(c)



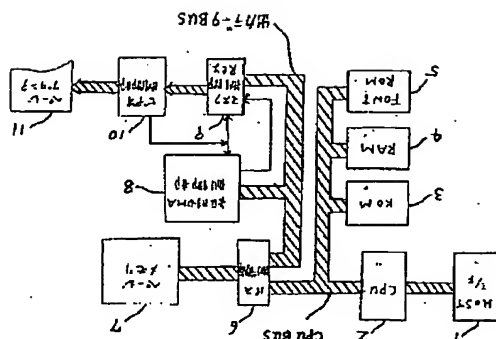
[Drawing 3]



[Drawing 4]



[Translation done.]



(57) 【要約】

【目的】 ハージメモリ上の任意の位置の矩形画像データをリソタにDM転送することにより、CPUの負担を減らし、トータルスループットを向上させることにある。

【構成】 CPUはビット表現でハージメモリ上の任意の矩形領域のアドレスを矩形DMA制御部に設定し、この矩形DMA制御部でX方向の始点、終点からアドレス及び有効ビットを求め、矩形領域のメモリだけをアクセスする方式である。

(54) 【発明の名称】 画像矩形DMA方式

(21) 出願番号	特願平4-31412	(71) 出願人	000003115 東洋電機製造株式会社
(22) 出願日	平成4年(1992)1月22日	(72) 発明者	武本 好徳 東京都中央区八重洲2丁目7番2号
		(72) 発明者	園村 諒将 神奈川県海老名市東柏ヶ谷四丁目6番32号 東洋電機製造株式会社相模工場内
		(72) 発明者	馬場 一郎 神奈川県海老名市東柏ヶ谷四丁目6番32号 東洋電機製造株式会社相模工場内

審査請求 未請求 請求項の数2(全7頁)

(51) Int. Cl. ⁶	識別記号	片内整理番号	F I	技術表示箇所
B 4 1 J 5/30	Z	8907-2C		
29/38	Z	8804-2C		
G 0 6 F 15/64	E	8840-5L		
H 0 4 N 1/387		4226-5C		

(43)公開日 平成5年(1993)8月3日

5-193203

台銀國際匯兌提款(II)

(12) 公關特許公報 (A)

(19) 日本国特許庁 (J P)

【0009】これらのアドレスは、実路上のページメモリ上においては先端アドレスは

$$(x_1 + 1) y_1 + m, \text{ 終端アドレスは } (x_1 + 1) y_2 + m_2$$

で表される。但し、 x 方向に関しては $\alpha \neq 0, \beta \neq 0$ の場合、 x_1, x_2 のアドレスの有効ビット数は各々 $(8 - \alpha), \beta$ となる。また、 $\beta = 0$ の場合、終端アドレスは

$$x_1(8 - \alpha)$$

を示す。

【0010】これらのアドレスは、実際にページメモリ上のアドレスとして用いられる。ここで、 m_1 は任意な値における先端アドレス、 m_2 は任意な値における終端アドレスを示す。

【0011】以上のようにして、図1の有効値である斜線部分7aが検出される。ページメモリ7に対するアドレスは、 x カウツタ、 y カウツタの値が各々Lower, Upperアドレスになるか、前述の有効範囲のみメモリーコントロールユニットはこの点でも向上する。図4は図1で示した x 方向の始点、終点部の有効ビットを決定する論理回路によって説明する。

図3は x 方形DMA制御部のブロック図であり、矩形の斜線部分7aの先端アドレス (x_1, y_1) 、終端アドレス (x_2, y_2) 、およびページメモリ7の終端アドレス x_m がセットされると、まずDMAはByte転送の為、各々の割り算器12、16にてByteに変換される。各々のMASR Bit $(x_i / 8)$ の下位3 Bit $(x_i / 8)$ の下位3 Bitについては、図1で説明した様に、有効ビット数の処理に使用される。但し $(x_2 / 8)$ の下位3 Bit $= 0$ の場合、減算器18により前述の終端アドレス $(x_m + 1) y_2 + m_2 - 1$ の処理をする為、比較器19には $(x_2 / 8) - 1$ の値がセットされる。そして、CPLよりこの制御部に起動信号であるGOF/Fがセットされ、ビチオ制御部10より画像同期信号であるXCLKが入力されてくると、カウツタ14が動き、 x 方向の有効値を比較器13によりカウツタ値が $(x_1 / 8)$ より大きいかあるいは等しいかをサーチする。 x カウツタ14の値が x と等しくなると、 y カウツタ20を1カウツアップする。 y 方向の有効値も比較器21によりカウツタ値が y_1 より大きいあるいは等しいかで有効となる。そして、 x 方向の終点は比較器19で検出される。同様に y_2 の終点

(3)

特圖平5-193203

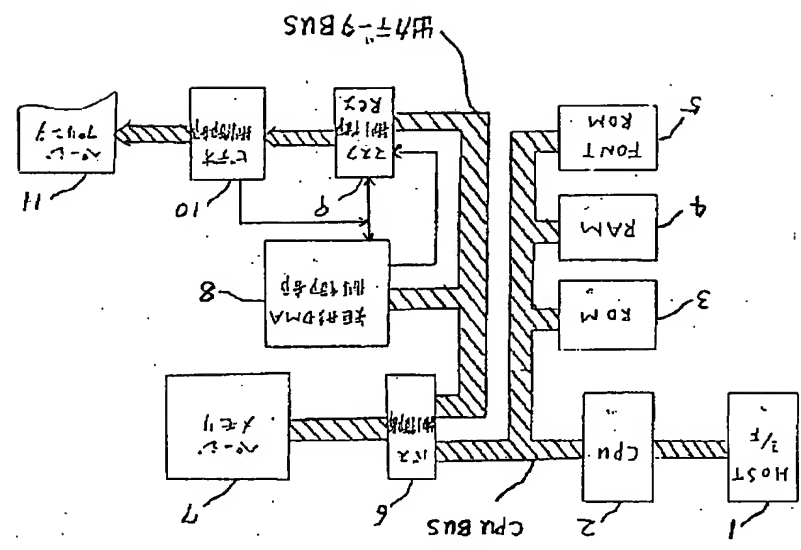
るフロッグ図であり、始点の場合下位3ビットは、8ビットに変換する為にx, M S K S E Tのタイミングでテスト24に入力され、出力は反転され(有効ビット8- α)、ゲート回路25のゲートを通じてレジスタ30にアイオライト信号(1/O)のタイミングで8ビットのレジスタ30にセットされる。X, M S K S E Tが偽の場合(x方向の始点でない場合)、ゲート回路26を通じてレジスタ30にセットされる。x方向の終点の場合、(x \searrow 下位3ビットはX, M S Kのタイミングでテスト27を通じて8ビットに変換され、出力はそのままで(有効ビット β)ゲート回路28を通じてレジスタ30にセットされる。X, M S K S E Tが偽の場合(x方向の終点でない)、ゲート回路25を通じてレジスタ30にセットされる。

【發明の效果】以上説明したごとく本發明によれば、ベ
ージング用のベージモリよりＣＰＵの介在なしに
ベージモリ上に作成されたデータを高速にベージリ
ングにDMA転送でき、かつ必要な矩形部分のみのデー
タをベージモリ上アウツセスする為トータルスリー
プは極めて大となる。又、任意の矩形バクメータのデー
タの区切りはバク単位でなくビット単位である為、バ
ク単位的にバク単位のアウツセングが可能となる為、バ
クスルアスリープト及びＣＰＵの負荷が減少できる。

【図面の簡単な説明】
 【図1】図1は有効画像データが格納されるベージメモリのイメージ図である。
 【図2】図2(a)，(b)，(c)は本実施例の画像矩形DMA転送方式の構成を示すブロック図である。
 【図3】図3は実施例における矩形DMA制御及びベージメモリアドレス生成を行なうブロック図である。
 【図4】図4は実施例におけるベージメモリ上のx方向の始点及び終点の有効ビットを決定するブロック図であ

【0014】
【符号の説明】

1	システム部
2	CPU
3	ROM
4	RAM
5	FONTROM
6	バス制御部
7	ペーシメモリ
8	矩形DMA制御部
9	マス制御レジスタ
10	ビデオ制御部
11	ペーシマリック

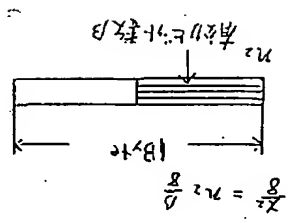


【図1】

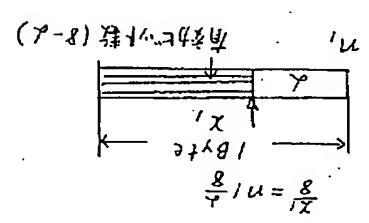
(4)

特開平5-193203

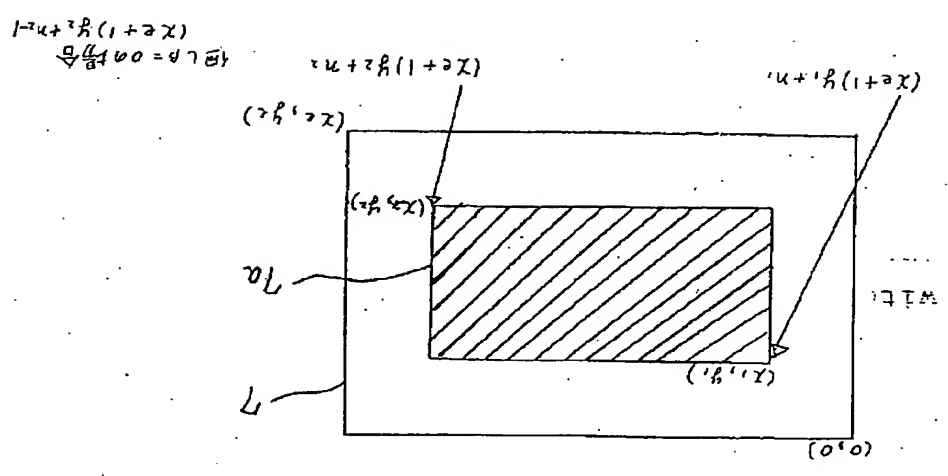
FIG



(c)

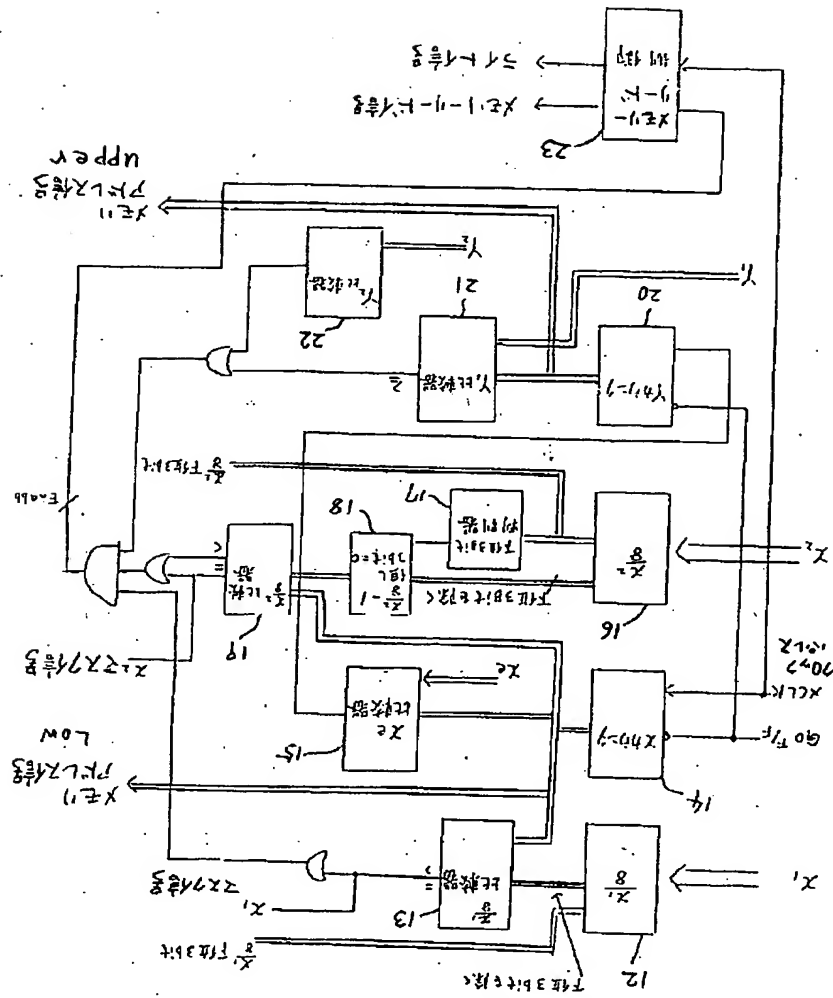


(b)

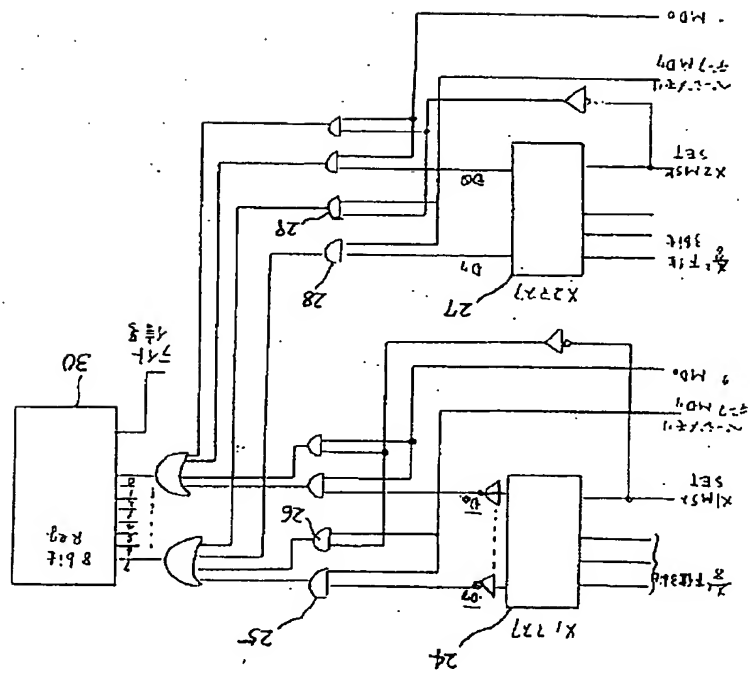


(a)

【図2】



【図3】



【図4】